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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/769,996	02/02/2004	Wei An	A0312.70497US00	2149

7590 03/05/2007

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EXAMINER	
HUANG, DAVID S	
ART UNIT	PAPER NUMBER
2609	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)
	10/769,996	AN ET AL.
	Examiner	Art Unit
	David Huang	2609

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 2 February 2004.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-24 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-24 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 02 February 2004 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 7/19/04 5/18/05

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The references listed in the Information Disclosure Statements filed on July 19, 2004 and May 18, 2005 have been considered by the examiner (see attached PTO-1449 form or PTO/SB/08A and 08B forms).

Drawings

2. The drawings are objected to because they are informal. In particular, the handwritten text the flow chart of Figure 4 is difficult to read; Figure 9A has a shaded region in element 302 that renders in unreadable; Figure 10 also contains shaded areas that make it difficult to read the labels; and Figure 11 contains shades that may not be reproduced accurately. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and

informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1-4, 7, 9-10, 13-16, 19, 21-22 and 24** are rejected under 35 U.S.C. 102(e) as being anticipated by Levin (US Patent Number 6,639,906).

Regarding **claim 1**, Levin discloses a method for processing a spread spectrum (system and method for performing digital receive processing, Abstract, lines 1-2; and each reverse link signal is modulated and demodulated with a set of PN codes in accordance with CDMA techniques, column 5, lines 28-30) baseband signal (receiver 102 filters, downconverts and digitizes a 1.25 MHz band of the RF energy that includes the set of reverse link signals, column 4, lines 60-67; where receiver 102 generates the baseband signal), comprising:

despreading samples of the baseband signal (demodulator 112 retrieves samples from circular buffer RAM 106 and despreads a set of reverse link signals stored therein, column 5, lines 24-28; Figure 4) with two or more instances of a spreading code (the same PN code segment is used to demodulate up to four instances of a particular reverse link signal, column 8, lines 45-46), the instances of the spreading code successively offset relative to the signal samples, to provide two or more despread results (each XOR bank 204-210 receives the PN code being decovered and applies the PN code to the samples at offsets of ½ the duration of a

spreading chip from one another yielding 0.0, 0.5, 1.0, and 1.5 chip offset despread data, column 8, lines 29-39, Figure 4); and

interpolating the two or more despread results (on-time interpolation circuit 214 receives both 0.5 chip offset despread data and 1.0 chip offset despread data, and calculates a value for on-time despread data at an offset of 0.5, 0.625, 0.75, or 0.875 using interpolation, column 9, lines 12-16) based on an estimated finger location (depending on the current offset of the finger being processed, column 9, lines 16-17) to provide a symbol estimate (demod FHT bank 116 receives the on-time despread data from demodulator 112 and generates on-time soft decision data, column 6, lines 13-16).

Regarding **claim 2**, Levin discloses everything claimed as applied above (see *claim 1*), and further discloses wherein the samples of the baseband signal are oversampled at two to four times a chip rate (digitized samples are provided at two (2) times the spreading chip rate, column 4, line 67 – column 5, line 1).

Regarding **claim 3**, Levin discloses everything claimed as applied above (see *claim 2*), and further discloses wherein the step of interpolating the two or more despread results produces an effective sampling of the baseband signal at eight times the chip rate (early interpolation circuit 212 calculates a value for a despread data offset by 0, 0.125, 0.25, or 0.375 of the duration of a chip (intervals of 1/8th the chip duration) before the current offset using interpolation, column 8, line 64 – column 9, line 3).

Regarding **claim 4**, Levin discloses everything claimed as applied above (see *claim 1*), and further discloses wherein interpolating the two or more despread results includes selecting the despread results around the estimated finger location (on-time interpolation circuit 214

calculates a value for on-time despread data at an offset of 0.5, 0.625, 0.75, or 0.875 using interpolation depending on the current offset of the finger being processed, column 9, lines 12-17; note that finger offset corresponds to finger location in time).

Regarding **claim 7**, Levin discloses everything claimed as applied above (see *claim 1*), and further discloses wherein the step of interpolating the two or more despread results is repeated at a symbol rate (during each Walsh symbol, system PN code generator 115 provides 72 bits of system PN code data to demodulator PN code generator 114, and demodulator 112 demodulates a set of reverse link signals using the PN codes supplied by demodulator PN code generator 114, column 8, lines 2-11; since interpolation circuits 212, 214, and 216 receive despread data from XOR banks 204-210 that demodulate up to four instances of a particular reverse link signal before the PN code for the next reverse link signal is latched, column 8, lines 40-46, the interpolation occurs for each set of despread data during each Walsh symbol, a symbol rate).

Regarding **claim 9**, Levin discloses everything claimed as applied above (see *claim 1*), and further discloses wherein successive instances of the spreading code are offset by one half chip relative to the signal samples (applies the PN code to the samples at offsets of ½ the duration of a spreading chip from one another, column 8, lines 33-35).

Regarding **claim 10**, Levin discloses everything claimed as applied above (see *claim 1*), and further discloses wherein the steps of despreading samples of the baseband signal and interpolating the two or more despread results are performed by a programmable digital signal processor (digital processing system 104 exchanges control data with an external control system

preferably comprised of a microprocessor running software stored in memory, column 4, lines 50-53).

Regarding **claim 13**, Levin discloses an apparatus for processing a spread spectrum (system and method for performing digital receive processing, Abstract, lines 1-2; and each reverse link signal is modulated and demodulated with a set of PN codes in accordance with CDMA techniques, column 5, lines 28-30) baseband signal (receiver 102 filters, downconverts and digitizes a 1.25 MHz band of the RF energy that includes the set of reverse link signals, column 4, lines 60-67; where receiver 102 generates the baseband signal), comprising:

means for despreading samples of the baseband signal (demodulator 112 retrieves samples from circular buffer RAM 106 and despreads a set of reverse link signals stored therein, column 5, lines 24-28; Figure 4) with two or more instances of a spreading code (the same PN code segment is used to demodulate up to four instances of a particular reverse link signal, column 8, lines 45-46), the instances of the spreading code successively offset relative to the signal samples, to provide two or more despread results (each XOR bank 204-210 receives the PN code being decovered and applies the PN code to the samples at offsets of ½ the duration of a spreading chip from one another yielding 0.0, 0.5, 1.0, and 1.5 chip offset despread data, column 8, lines 29-39, Figure 4); and

means for interpolating the two or more despread results (on-time interpolation circuit 214 receives both 0.5 chip offset despread data and 1.0 chip offset despread data, and calculates a value for on-time despread data at an offset of 0.5, 0.625, 0.75, or 0.875 using interpolation, column 9, lines 12-16) based on an estimated finger location (depending on the current offset of the finger being processed, column 9, lines 16-17) to provide a symbol estimate (demod FHT

bank 116 receives the on-time despread data from demodulator 112 and generates on-time soft decision data, column 6, lines 13-16).

Regarding **claim 14**, Levin discloses everything claimed as applied above (see *claim 13*), and further discloses wherein the samples of the baseband signal are oversampled at two to four times a chip rate (digitized samples are provided at two (2) times the spreading chip rate, column 4, line 67 – column 5, line 1).

Regarding **claim 15**, Levin discloses everything claimed as applied above (see *claim 14*), and further discloses wherein the means for interpolating the two or more despread results performs an effective sampling of the baseband signal at eight times the chip rate (early interpolation circuit 212 calculates a value for a despread data offset by 0, 0.125, 0.25, or 0.375 of the duration of a chip (intervals of 1/8th the chip duration) before the current offset using interpolation, column 8, line 64 – column 9, line 3).

Regarding **claim 16**, Levin discloses everything claimed as applied above (see *claim 13*), and further discloses wherein the means for interpolating the two or more despread results includes means for selecting the despread results around the estimated finger location (on-time interpolation circuit 214 calculates a value for on-time despread data at an offset of 0.5, 0.625, 0.75, or 0.875 using interpolation depending on the current offset of the finger being processed, column 9, lines 12-17; note that finger offset corresponds to finger location in time).

Regarding **claim 19**, Levin discloses everything claimed as applied above (see *claim 13*), and further discloses wherein the means for interpolating the two or more despread results operates at a symbol rate (during each Walsh symbol, system PN code generator 115 provides 72 bits of system PN code data to demodulator PN code generator 114, and demodulator 112

demodulates a set of reverse link signals using the PN codes supplied by demodulator PN code generator 114, column 8, lines 2-11; since interpolation circuits 212, 214, and 216 receive despread data from XOR banks 204-210 that demodulate up to four instances of a particular reverse link signal before the PN code for the next reverse link signal is latched, column 8, lines 40-46, the interpolation occurs for each set of despread data during each Walsh symbol, a symbol rate).

Regarding **claim 21**, Levin discloses everything claimed as applied above (see *claim 13*), and further discloses wherein successive instances of the spreading code are offset by one half chip relative to the signal samples (applies the PN code to the samples at offsets of ½ the duration of a spreading chip from one another, column 8, lines 33-35).

Regarding **claim 22**, Levin discloses everything claimed as applied above (see *claim 13*), and further discloses wherein the means for despreading and the means for interpolating are implemented by a programmable digital signal processor (digital processing system 104 exchanges control data with an external control system preferably comprised of a microprocessor running software stored in memory, column 4, lines 50-53).

Regarding **claim 24**, Levin discloses an apparatus for processing a spread spectrum (system and method for performing digital receive processing, Abstract, lines 1-2; and each reverse link signal is modulated and demodulated with a set of PN codes in accordance with CDMA techniques, column 5, lines 28-30) baseband signal signal (receiver 102 filters, downconverts and digitizes a 1.25 MHz band of the RF energy that includes the set of reverse link signals, column 4, lines 60-67; where receiver 102 generates the baseband signal), comprising:

a digital signal processor (digital processing system 104, Figure 4) including a memory for holding instructions (digital processing system 104 exchanges control data with a microprocessor running software stored in memory, column 4, lines 50-53) and data (digital samples are received by RAM interface 103 which stores the 2xsamples in antenna interface circular buffer RAM 106, column 5, lines 8-10), program sequencer for controlling execution of an instruction sequence (control system 110, Figure 4) and at least one computation block for executing the instruction sequence (demodulator despreader 112 and demod FHT bank 116), said computation block including means for despreading samples of the baseband signal (XOR banks 204-210, Figure 5) with two or more instances of a spreading code (the same PN code segment is used to demodulate up to four instances of a particular reverse link signal, column 8, lines 45-46), the instances of the spreading code successively offset relative to the signal samples, to provide two or more despread results (each XOR bank 204-210 receives the PN code being decovered and applies the PN code to the samples at offsets of ½ the duration of a spreading chip from one another yielding 0.0, 0.5, 1.0, and 1.5 chip offset despread data, column 8, lines 29-39, Figure 4), and means for interpolating the two or more despread results (on-time interpolation circuit 214 receives both 0.5 chip offset despread data and 1.0 chip offset despread data, and calculates a value for on-time despread data at an offset of 0.5, 0.625, 0.75, or 0.875 using interpolation, column 9, lines 12-16) based on an estimated finger location (depending on the current offset of the finger being processed, column 9, lines 16-17) to provide a symbol estimate (demod FHT bank 116 receives the on-time despread data from demodulator 112 and generates on-time soft decision data, column 6, lines 13-16).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 5-6, 11-12, 17-18 and 23** rejected under 35 U.S.C. 103(a) as being unpatentable over Levin (US Patent 6,639,906).

Regarding **claim 5**, Levin discloses everything claimed as applied above (see *claim 4*), but fails to explicitly disclose wherein interpolating the two or more despread results comprises selecting interpolation coefficients based on the estimated finger location.

Levin does disclose the use of simple linear interpolation or any seven tap (coefficient/delay pair) FIR is appropriate for the early interpolation circuit 212 (column 9, lines 8-11). Levin also discloses early interpolation circuit 212 calculates a value for despread data offset by 0, 0.125, 0.25, or 0.375 of the duration of a chip before the current offset. In particular, early interpolation circuit 212 calculates a value for despread data offset by 0.5 relative to on-time interpolation circuit 214, and on-time interpolation circuit 214 calculates a value for on-time despread data using interpolation depending on the current offset of the finger being processed (column 9, lines 12-16), meaning early interpolation circuit 212 interpolates a value at one of the four offsets depending on the current offset or location of the finger being processed.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Levin's invention to select interpolation coefficients based on an

estimated finger location as claimed because Levin suggests the use of any seven tap FIR filter in early interpolation filter 212 where filter coefficients are inherent to the operation of FIR filters, and different coefficients are used depending on the desired offset.

Regarding **claim 6**, Levin discloses everything claimed as applied above (see *claim 5*), and further discloses wherein the step of interpolating the two or more despread results comprises multiplying the selected despread results by respective selected interpolation coefficients (on-time interpolation circuit 214 receives 0.0 and 0.5 chip offset despread data and calculates an interpolated value using an FIR filter, column 8, line 66 – column 9, line 11; note that it is inherent to an FIR filter to multiply samples with tap coefficients) to provide intermediate values (calculates a value for on-time dispread data, column 9, line 14) and summing the intermediate values (demod FHT bank 116 receives the on-time despread data from demodulator 112, and accumulates energy correlation vectors, column 9, lines 47-48; the originally received on-time despread data from demodulator 112 is processed within demod FHT 116 into a from accumulated by Accumulator 306, column 9, lines 31-50; see Figure 6) to provide the symbol estimate (Demod FHT bank 116 generates on-time soft decision data, column 6, lines 13-16).

Regarding **claim 11**, Levin discloses everything claimed as applied above (see *claim 10*), but fails to particularly disclose wherein the step of despreading samples of the baseband signal comprises performing a plurality of despreading operations simultaneously.

Levin does disclose each XOR bank receives the PN code being decovered and applies the PN code to the samples at offsets of ½ the duration of a spreading chip from one another yielding 0.0, 0.5, 1.0, and 1.5 chip offset despread data (column 8, lines 32-37; Figure 5), and

early, on-time and late interpolation circuits (212, 214, and 216, respectively; see Figure 5) each receive two sets offset despread data to calculate interpolated values (column 8, line 66 – column 9, line 30; see Figure 5). Furthermore, the same PN code segment is used to demodulate up to four instances of a particular reverse link signal.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Levin's invention to perform a plurality of dispreading operations simultaneously, as claimed, since the plurality of despread results must be received by the interpolation circuits at the same time to ensure proper operation and calculation of interpolated values and simultaneous dispreading operations would improve the efficiency of operation by taking full advantage of the parallel structure of the XOR banks.

Regarding **claim 12**, Levin discloses everything claimed as applied above (see *claim 1*), but fails to explicitly disclose wherein interpolating the two or more despread results comprises:

interpolating the two or more despread results using interpolation coefficients corresponding to the estimated finger location,

interpolating the two or more despread results using interpolation coefficients corresponding to a time earlier than the estimated finger location, and

interpolating the two or more despread results using interpolation coefficients corresponding to a time later than the estimated finger location.

Nevertheless, Levin does disclose on-time interpolation circuit 214 receives 0.5 and 1.0 chip offset despread data, and calculates a value for on-time despread data at an offset of 0.5, 0.625, 0.75, or 0.875 (at offsets of intervals of $1/8^{th}$ the chip duration) of using interpolation, depending on the current offset of the finger being processed (column 9, lines 12-17). Early

interpolation circuit 212 receives 0.0 and 0.5 chip offset despread data and calculates a value for despread data offset by 0.5 relative to on-time interpolation circuit 214 (column 8, lines 66-67 and column 9, lines 3-6). Late interpolation circuit receives 1.0 and 1.5 chip offset despread data and calculates a value for despread data delayed 0.5 the duration of a spreading chip from on-time despread data (column 9, lines 18-20 and 23-25). Levin also discloses the use of simple linear interpolation or any seven tap FIR is appropriate for implementing early interpolation circuit 212 (column 9, lines 8-11), and linear interpolation or a 15 tap FIR is suitable for implementing late interpolation circuit 216 (column 9, lines 26-30).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Levin's invention to implement on-time interpolation circuit 214 using an FIR filter as suggested by Levin for both early and late interpolation circuits 212 and 214, respectively, since interpolating values in the same way for all three interpolation circuits 212, 214, 216 would reduce development time. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use interpolation coefficients corresponding to the estimated finger location for interpolation circuits 212, 214, and 216 because the circuits calculate interpolated values at one of four offsets and require different coefficients for each offset.

Regarding **claim 17**, Levin discloses everything claimed as applied above (*claim 16*), but fails to explicitly disclose wherein the means for interpolating the two or more despread results comprises means for selecting interpolation coefficients based on the estimated finger location.

Levin does disclose the use of simple linear interpolation or any seven tap (coefficient/delay pair) FIR is appropriate for the early interpolation circuit 212 (column 9, lines

8-11). Levin also discloses early interpolation circuit 212 calculates a value for despread data offset by 0, 0.125, 0.25, or 0.375 of the duration of a chip before the current offset. In particular, early interpolation circuit 212 calculates a value for despread data offset by 0.5 relative to on-time interpolation circuit 214, and on-time interpolation circuit 214 calculates a value for on-time despread data using interpolation depending on the current offset of the finger being processed (column 9, lines 12-16), meaning early interpolation circuit 212 interpolates a value at one of the four offsets depending on the current offset or location of the finger being processed.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Levin's invention with means for selecting interpolation coefficients based on an estimated finger location as claimed because Levin suggests the use of any seven tap FIR filter in early interpolation filter 212 where filter coefficients are inherent to the operation of FIR filters, and different coefficients are used depending on the desired offset.

Regarding **claim 18**, Levin discloses everything claimed as applied above (see *claim 17*), and further discloses wherein the step of interpolating the two or more despread results comprises multiplying the selected despread results by respective selected interpolation coefficients (on-time interpolation circuit 214 receives 0.0 and 0.5 chip offset despread data and calculates an interpolated value using an FIR filter, column 8, line 66 – column 9, line 11; note that it is inherent to an FIR filter to multiply samples with tap coefficients) to provide intermediate values (calculates a value for on-time dispread data, column 9, line 14) and summing the intermediate values (demod FHT bank 116 receives the on-time despread data from demodulator 112, and accumulates energy correlation vectors, column 9, lines 47-48; the originally received on-time despread data from demodulator 112 is processed within demod FHT

116 into a from accumulated by Accumulator 306, column 9, lines 31-50; see Figure 6) to provide the symbol estimate (Demod FHT bank 116 generates on-time soft decision data, column 6, lines 13-16).

Regarding **claim 23**, Levin discloses everything claimed as applied above (*claim 22*), but fails to particularly disclose wherein the means for despreading samples of the baseband signal comprises means for performing a plurality of despreading operations simultaneously.

However, Levin does disclose each XOR bank receives the PN code being decovered and applies the PN code to the samples at offsets of ½ the duration of a spreading chip from one another yielding 0.0, 0.5, 1.0, and 1.5 chip offset despread data (column 8, lines 32-37; Figure 5), and early, on-time and late interpolation circuits (212, 214, and 216, respectively; see Figure 5) each receive two sets offset despread data to calculate interpolated values (column 8, line 66 – column 9, line 30; see Figure 5). Furthermore, the same PN code segment is used to demodulate up to four instances of a particular reverse link signal.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Levin's invention to perform a plurality of dispreading operations simultaneously, as claimed, since the plurality of despread results must be received by the interpolation circuits at the same time to ensure proper operation and calculation of interpolated values and simultaneous dispreading operations would improve the efficiency of operation by taking full advantage of the parallel structure of the XOR banks.

7. **Claims 8 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Levin (US Patent 6,639,906) in view of admitted prior art Komatsu (US Patent 6,816,542).

Regarding **claims 8 and 20**, Levin discloses everything claimed as applied above (see *claims 1 and 13*), and further discloses wherein despreading and means for despreading samples of the baseband signal comprises multiplying the samples by respective code elements (each XOR bank 204-210 receives the PN code being decovered and applies the PN code to the samples, column 8, lines 32-34) to provide intermediate values (yielding 0.0, 0.5, 1.0, and 1.5 chip offset despread data column 8, lines 34-36).

However, Levin fails to disclose accumulating the intermediate values to provide a despread result.

Nevertheless, Levin does teach that demod FHT bank 116 receives the on-time despread data from demodulator 112 (column 6, lines 13-14), 32x2 FHT 300 perform fast Hadamard transforms on in-phase (I) and quadrature phase (Q) components, adder-subtractor butterfly combiner 308 combines the output from the even and odd samples yielding an I correlation vector and a Q correlation vector (column 9, lines 33-35 and 40-43). I-Q dot product 304 generates the dot product of the I and Q correlation vectors yield a correlation energy vector that is forwarded to accumulator 306 which accumulates the energy correlation vectors from I-Q dot product 304 (column 9, lines 47-49).

Komatsu discloses interpolative despreader 5 comprising received signal shift register 21, spreading code register 22, multipliers 23, and adder 24. Received signal shift register 21 shifts received signals received by interpolative despreader 5. Spreading code register 22 sets a spreading code sequence of the same bit length as received signal shift register 21. Multipliers 23 multiply the values of received signal shift register 21 and spreading code register 22

together. Adder 24 adds together the output signals of multipliers 23 (column 4, lines 38-47;see Figure 7).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Levin's invention to accumulate intermediate values as taught be Komatsu because this would reduce the complexity of the invention by allowing accumulation without having to process the intermediate symbols in demod FHT bank 116.

Citation of Pertinent Prior Art

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Cheung et al. (US Patent Application Publication US 2003/0142639) disclose a pilot searcher for CDMA and GPS signals implemented with a digital signal processor.

Ding et al. (US Patent 6,839,380) disclose an effective synchronization technique for an embedded signaling system based on direct sequence spread spectrum technology implemented in a digital signal processor.

Easton et al. (US Patent 6,985,516) disclose a method and apparatus for processing a received signal in a communications system that interpolates despread samples to generate interpolated samples.

Mukai et al. (US Patent Application Publication US 2003/0181218) disclose a radio communication apparatus which receives and processes radio signals using programmable hardware circuits.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Huang whose telephone number is (571) 270-1798. The examiner can normally be reached on Monday - Friday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eliseo Ramos-Feliciano can be reached on (571) 272-7925. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DSH/dsh

2/21/07
ELISEO RAMOS-FELICIANO
SUPERVISORY PATENT EXAMINER